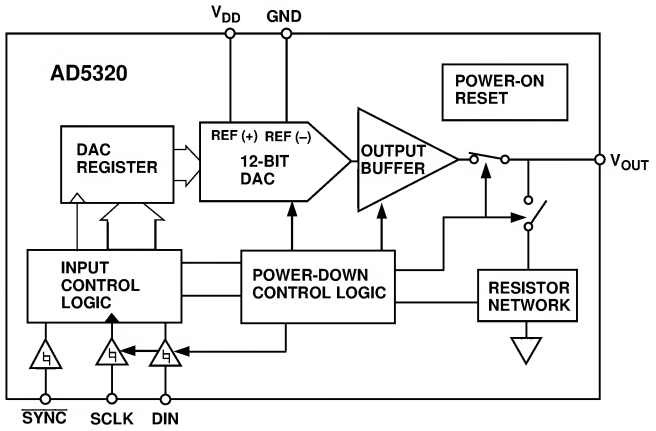
+2.7 V to +5.5 V, 140 μA, Rail-to-Rail Voltage Output 12-Bit DAC

AD5320*

FEATURES
Single 12-Bit DAC
6-Lead SOT-23 and 8-Lead microSOIC Packages
Micropower Operation: 140 μA @ 5 V
Power-Down to 200 nA @ 5 V, 50 nA @ 3 V
+2.7 V to +5.5 V Power Supply
Guaranteed Monotonic by Design
Reference Derived from Power Supply
Power-On-Reset to Zero Volts
Three Power-Down Functions
Low Power Serial Interface with Schmitt-Triggered Inputs
On-Chip Output Buffer Amplifier, Rail-to-Rail Operation
$\overline{\text{SYNC}}$ Interrupt Facility

APPLICATIONS
Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5320 is a single, 12-bit voltage out DAC that operates from a single +2.7 V to +5.5 V supply. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The AD5320 utilizes a versatile three-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™ and DSP interface standards.

The reference for AD5320 is derived from the power supply inputs and thus gives the widest dynamic output range. The part incorporates a power-on-reset circuit that ensures that the DAC output powers up to zero volts and remains there until a valid write takes place to the device. The part contains a power-down feature that reduces the current consumption of the device to typically 200 nA at 5 V and provides software selectable output loads while in power-down mode. The part is put into power-down mode over the serial interface.

The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The power consumption is 0.7 mW at 5 V reducing to 1 μW in power-down mode.

The AD5320 is available in a 6-lead SOT-23 package and an 8-lead microSOIC package.

PRODUCT HIGHLIGHTS

1. Low power, single supply operation. This part operates from a single +2.7 V to +5.5 V supply and typically consumes 0.35 mW at 3 V and 0.7 mW at 5 V, making it ideal for battery powered applications.
2. The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a slew rate of 1 V/μs.
3. Reference derived from the power supply.
4. High speed serial interface with clock speeds up to 30 MHz.
5. Power-down capability. When powered down, the DAC typically consumes 50 nA at 3 V and 200 nA at 5 V.

SPI and QSPI are trademarks of Motorola.
MICROWIRE is a trademark of National Semiconductor.
*Patent pending; protected by U.S. Patent No. 5684481.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD5320–SPECIFICATIONS (V_{DD} = +2.7 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version[1] Min	Typ	Max	Units	Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	12			Bits	
Relative Accuracy			±16	LSB	See Figure 2.
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic by Design. See Figure 3.
Zero Code Error		+5	+40	mV	All Zeroes Loaded to DAC Register. See Figure 6.
Full-Scale Error		–0.15	–1.25	% of FSR	All Ones Loaded to DAC Register. See Figure 6.
Gain Error			±1.25	% of FSR	
Zero Code Error Drift		–20		µV/°C	
Gain Temperature Coefficient		–5		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time		8	10	µs	1/4 Scale to 3/4 Scale Change (400 Hex to C00 Hex). See Figure 16.
Slew Rate		1		V/µs	
Digital-to-Analog Glitch Impulse		20		nV-s	1 LSB Change Around Major Carry. See Figure 19.
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1		Ω	
Short Circuit Current		50		mA	V_{DD} = +5 V
		20		mA	V_{DD} = +3 V
Power-Up Time		2.5		µs	Coming Out of Power-Down Mode. V_{DD} = +5 V
		5		µs	Coming Out of Power-Down Mode. V_{DD} = +3 V
LOGIC INPUTS[3]					
Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.8	V	V_{DD} = +5 V
V_{INL}, Input Low Voltage			0.6	V	V_{DD} = +3 V
V_{INH}, Input High Voltage	2.4			V	V_{DD} = +5 V
V_{INH}, Input High Voltage	2.1			V	V_{DD} = +3 V
Pin Capacitance			3	pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)					DAC Active and Excluding Load Current
V_{DD} = +4.5 V to +5.5 V		140	250	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = +2.7 V to +3.6 V		115	200	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (Power-Down)					
V_{DD} = +4.5 V to +5.5 V		0.2	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = +2.7 V to +3.6 V		0.05	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}		93		%	I_{LOAD} = 2 mA. V_{DD} = +5 V

NOTES
[1]Temperature ranges are as follows: B Version: –40°C to +105°C.
[2]Linearity calculated using a reduced code range of 48 to 4047. Output unloaded.
[3]Guaranteed by design and characterization, not production tested.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +2.7 V to +5.5 V; GND = 0 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	0	ns min	$\overline{SYNC}$ to SCLK Active Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_8	33	ns min	Minimum $\overline{SYNC}$ High Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2]See Figure 1.

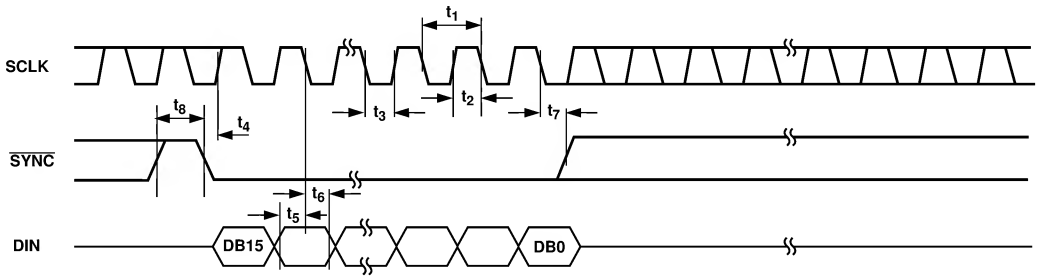


Figure 1. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +7 V
Digital Input Voltage to GND ..... –0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) ..... –40°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
SOT-23 Package
  θ_{JA} Thermal Impedance ..... 240°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
microSOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 206°C/W
  θ_{JC} Thermal Impedance ..... 44°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Options*
AD5320BRT	–40°C to +105°C	RT-6
AD5320BRM	–40°C to +105°C	RM-8

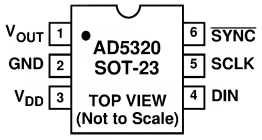
*RT = SOT-23; RM = microSOIC.

CAUTION

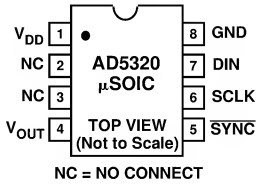
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5320 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

SOT-23



microSOIC



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

SOT-23 Pin Numbers

Pin No.	Mnemonic	Function
1	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
2	GND	Ground reference point for all circuitry on the part.
3	V_{DD}	Power Supply Input. These parts can be operated from +2.5 V to +5.5 V and should be decoupled to GND.
4	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
5	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
6	$\overline{SYNC}$	Level triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless $\overline{SYNC}$ is taken high before this edge in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write signal is ignored by the DAC.

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 2.

Differential Nonlinearity
Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 3.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (000 Hex) is loaded to the DAC register. Ideally the output should be 0 V. The zero-code error is always positive in the AD5320 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 6.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (FFF Hex) is loaded to the DAC register. Ideally the output should be V_{DD} – 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 6.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error
Total Unadjusted Error (TUE) is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure 4.

Zero-Code Error Drift
This is a measure of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (7FF Hex to 800 Hex).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC output from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

AD5320- Typical Performance Characteristics

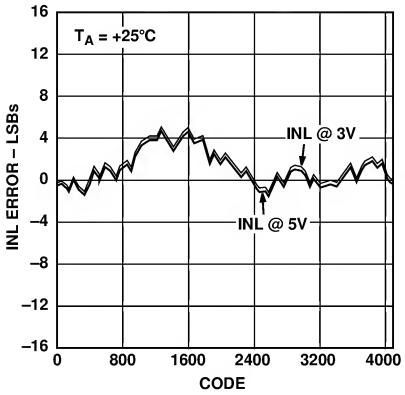


Figure 2. Typical INL Plot

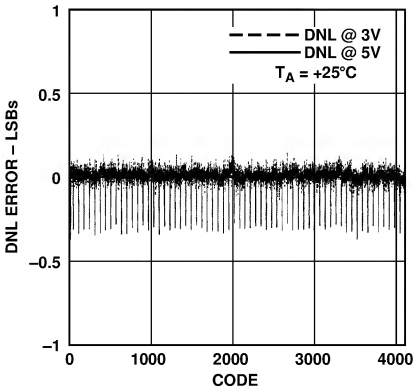


Figure 3. Typical DNL Plot

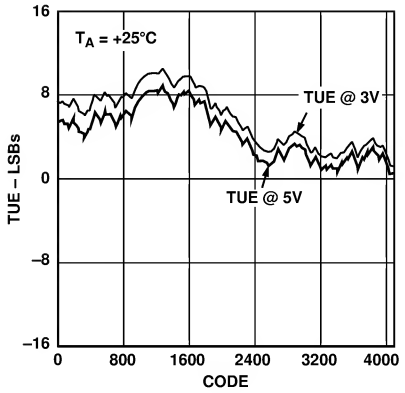


Figure 4. Typical Total Unadjusted Error Plot

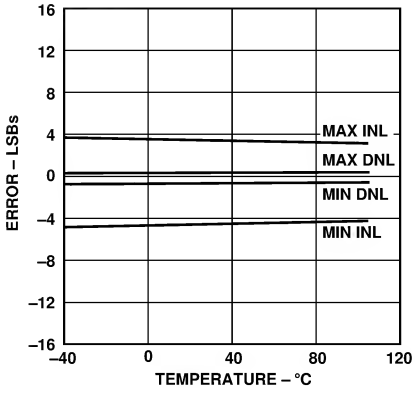


Figure 5. INL Error and DNL Error vs. Temperature

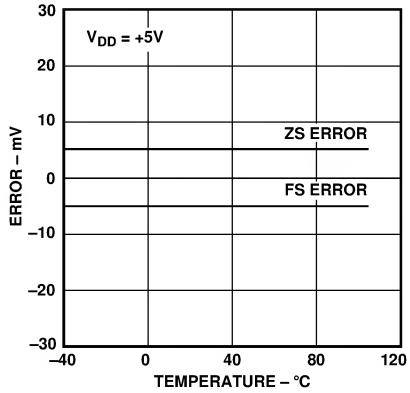


Figure 6. Zero-Scale Error and Full-Scale Error vs. Temperature

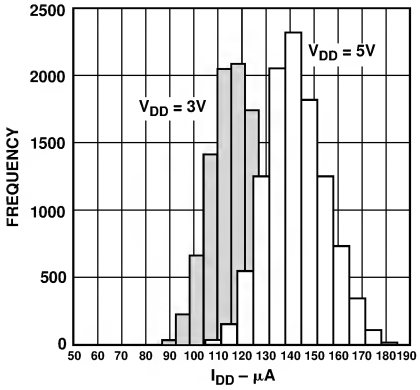


Figure 7. I_{DD} Histogram with V_{DD} =3 V and V_{DD} =5 V

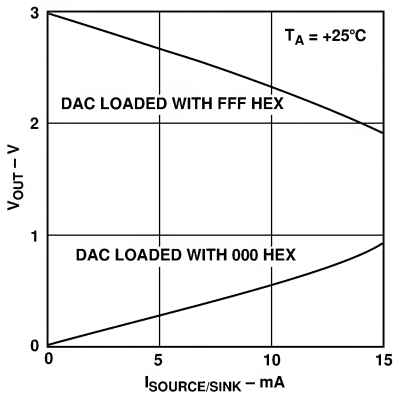


Figure 8. Source and Sink Current Capability with V_{DD} =3 V

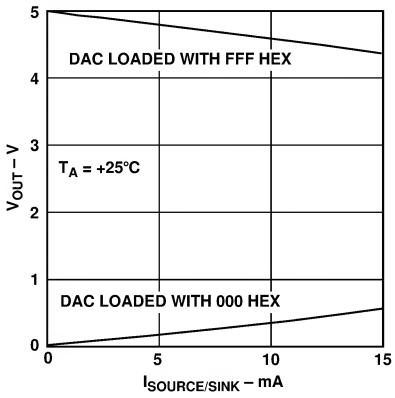


Figure 9. Source and Sink Current Capability with V_{DD} =5 V

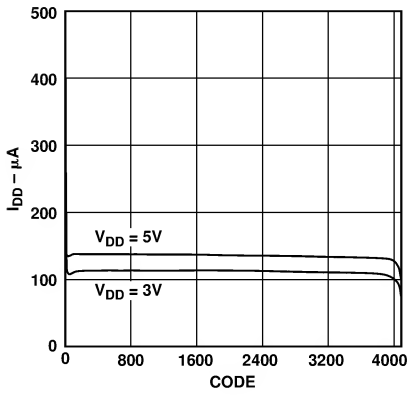


Figure 10. Supply Current vs. Code

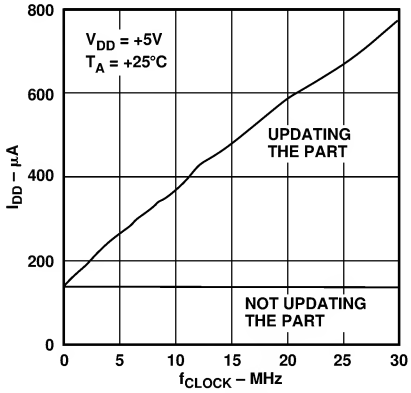


Figure 11. Supply Current vs. f_{CLOCK}

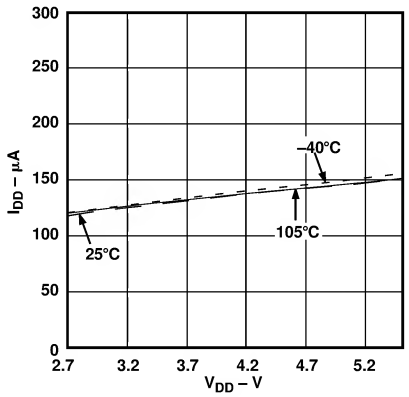


Figure 12. Supply Current vs. Supply Voltage

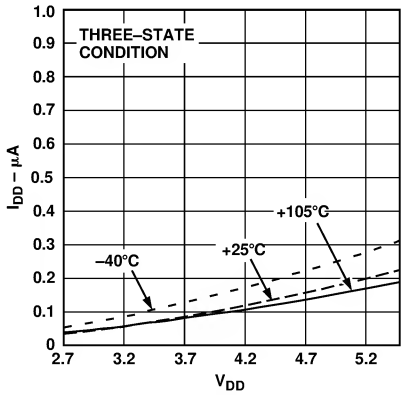


Figure 13. Power-Down Current vs. Supply Voltage

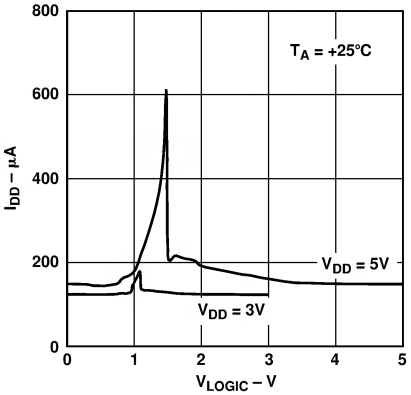


Figure 14. Supply Current vs. Logic Input Voltage

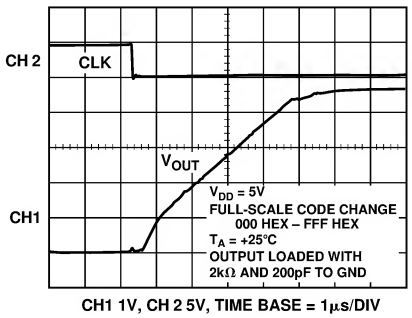


Figure 15. Full-Scale Settling Time

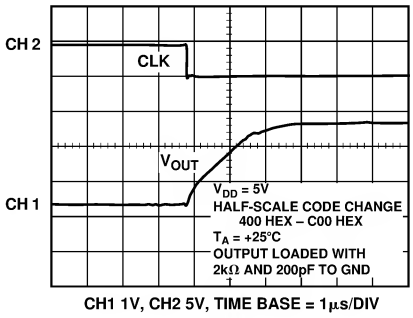


Figure 16. Half-Scale Settling Time

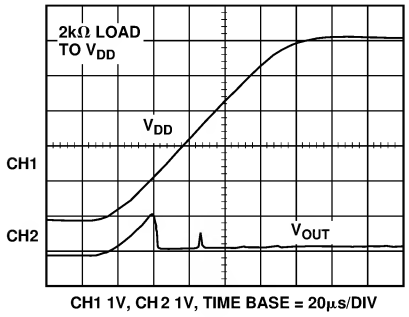


Figure 17. Power-On Reset to 0 V

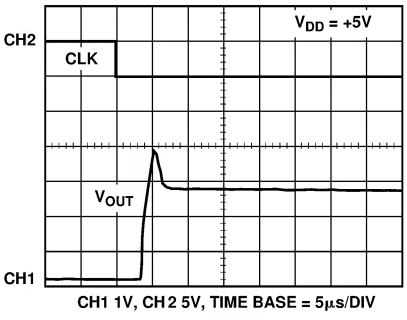


Figure 18. Exiting Power-Down (800 Hex Loaded)

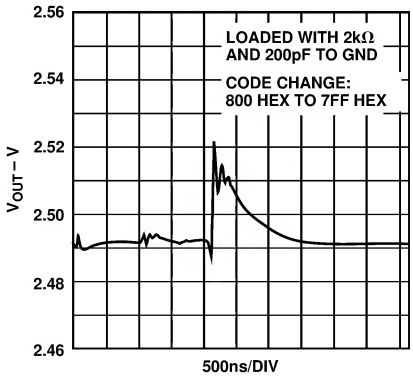


Figure 19. Digital-to-Analog Glitch Impulse

GENERAL DESCRIPTION

D/A Section

The AD5320 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Since there is no reference input pin, the power supply (V_{DD}) acts as the reference. Figure 20 shows a block diagram of the DAC architecture.

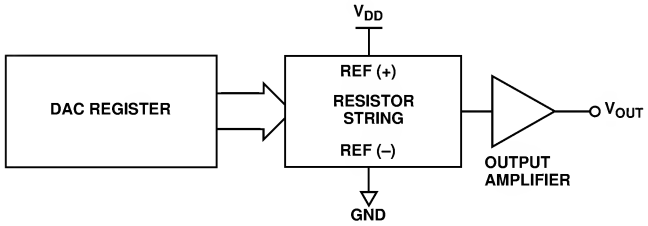


Figure 20. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{DD} \times \left(\frac{D}{4096} \right)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 4095.

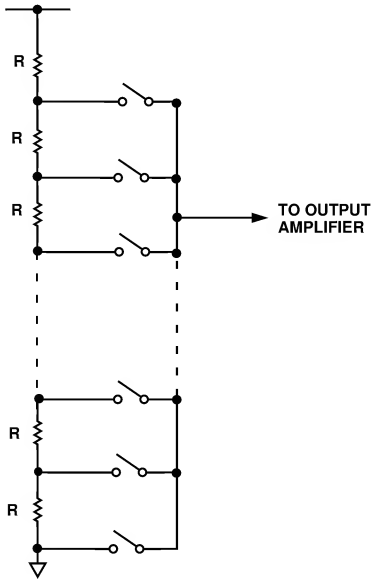


Figure 21. Resistor String

Resistor String

The resistor string section is shown in Figure 21. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 200 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figures 8 and 9. The slew rate is 1 V/μs with a half-scale settling time of 8 μs with the output unloaded.

SERIAL INTERFACE

The AD5320 has a three-wire serial interface ($\overline{SYNC}$, SCLK and DIN), which is compatible with SPI, QSPI and Microwire interface standards as well as most DSPs. See Figure 1 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5320 compatible with high speed DSPs. On the sixteenth falling clock edge, the last data bit is clocked in and the programmed function is executed (i.e. a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{SYNC}$ line may be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Since the $\overline{SYNC}$ buffer draws more current when V_{IN} = 2.4 V than it does when V_{IN} = 0.8 V, $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned above, however, it must be brought high again just before the next write sequence.

Input Shift Register

The input shift register is 16 bits wide (see Figure 22). The first two bits are "don't cares." The next two are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next twelve bits are the data bits. These are transferred to the DAC register on the sixteenth falling edge of SCLK.

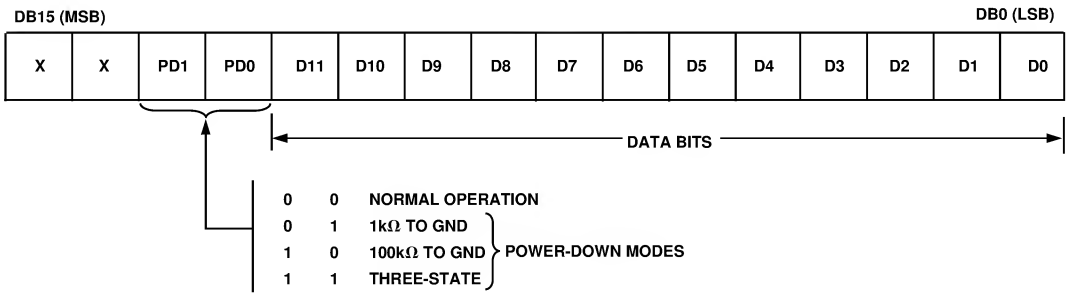


Figure 22. Input Register Contents

$\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs—see Figure 23.

Power-On-Reset

The AD5320 contains a power-on-reset circuit that controls the output voltage during power-up. The DAC register is filled with zeros and the output voltage is 0 V. It remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

Power-Down Modes

The AD5320 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB13 and DB12) in the control register. Table I shows how the state of the bits corresponds to the mode of operation of the device.

Table I. Modes of Operation for the AD5320

DB13	DB12	Operating Mode
0	0	Normal Operation Power-Down Modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-State

When both bits are set to 0, the part works normally with its normal power consumption of 140 μA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor or it is left open-circuited (Three-State). The output stage is illustrated in Figure 24.

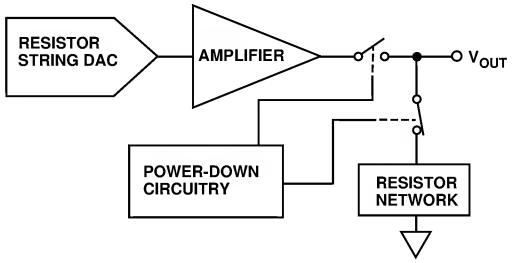


Figure 24. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs for V_{DD} = 3 V. See Figure 18 for a plot.

MICROPROCESSOR INTERFACING

AD5320 to ADSP-2101/ADSP-2103 Interface

Figure 25 shows a serial interface between the AD5320 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT Transmit Alternate Framing Mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active Low Framing, 16-Bit Word Length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

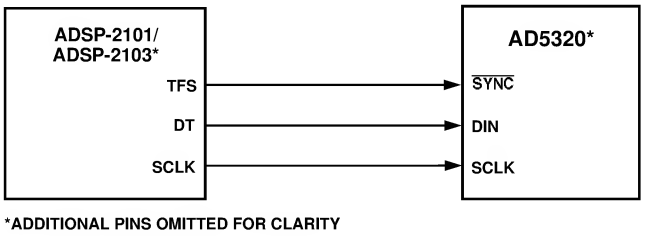


Figure 25. AD5320 to ADSP-2101/ADSP-2103 Interface

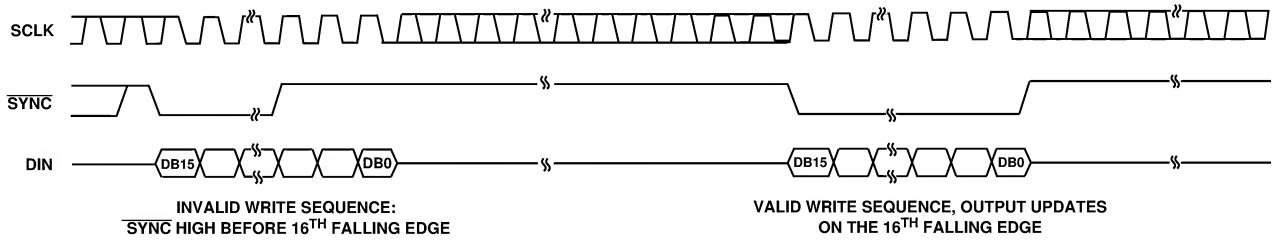


Figure 23. $\overline{\text{SYNC}}$ Interrupt Facility

AD5320 to 68HC11/68L11 Interface

Figure 26 shows a serial interface between the AD5320 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the CLKIN of the AD5320, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC, the $\overline{SYNC}$ line is taken low (PC7). When the 68HC11/68L11 is configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5320, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC and PC7 is taken high at the end of this procedure.

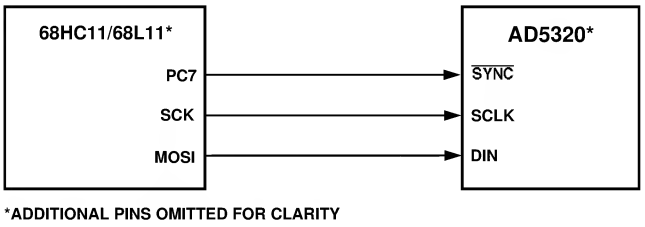


Figure 26. AD5320 to 68HC11/68L11 Interface

AD5320 to 80C51/80L51 Interface

Figure 27 shows a serial interface between the AD5320 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5320, while RXD drives the serial data line of the part. The $\overline{SYNC}$ signal is again derived from a bit programmable pin on the port. In this case port line P3.3 is used. When data is to be transmitted to the AD5320, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format which has the LSB first. The AD5320 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

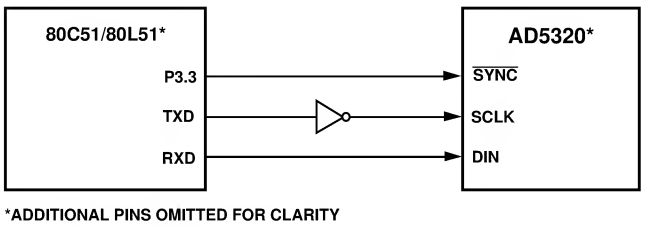


Figure 27. AD5320 to 80C51/80L51 Interface

AD5320 to Microwire Interface

Figure 28 shows an interface between the AD5320 and any microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5320 on the rising edge of the SK.

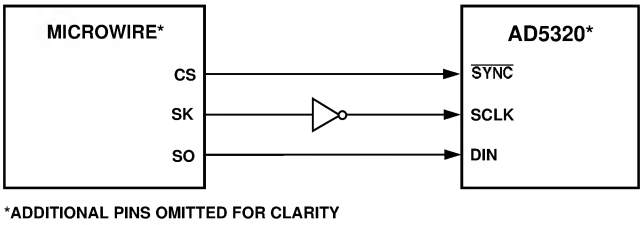


Figure 28. AD5320 to Microwire Interface

APPLICATIONS

Using REF19x as a Power Supply for AD5320

Because the supply current required by the AD5320 is extremely low, an alternative option is to use a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) to supply the required voltage to the part—see Figure 29. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V (e.g., 15 V). The REF19x will output a steady supply voltage for the AD5320. If the low dropout REF195 is used, the current it needs to supply to the AD5320 is 140 μA. This is with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is:

$$140\ \mu A + (5\ V/5\ k\Omega) = 1.14\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 2.3 ppm (11.5 μV) for the 1.14 mA current drawn from it. This corresponds to a 0.009 LSB error.

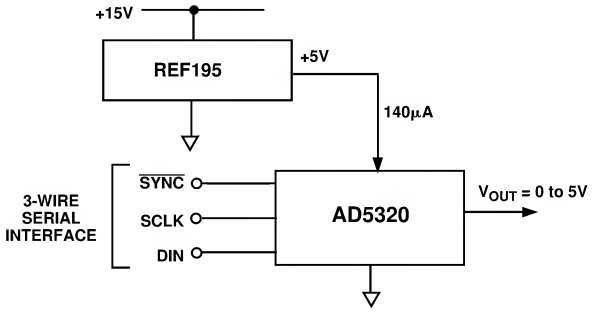


Figure 29. REF195 as Power Supply to AD5320

Bipolar Operation Using the AD5320

The AD5320 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 30. The circuit below will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{4096}\right) \times \left(\frac{R1+R2}{R1}\right) - V_{DD} \times \left(\frac{R2}{R1}\right)\right]$$

where D represents the input code in decimal (0–4095). With V_{DD} = 5 V, R1 = R2 = 10 kΩ:

$$V_O = \left(\frac{10 \times D}{4096}\right) - 5V$$

This is an output voltage range of ±5 V with 000 Hex corresponding to a –5 V output and FFF Hex corresponding to a +5 V output.

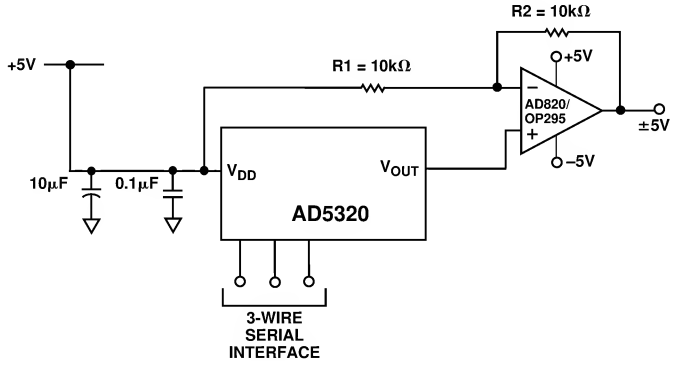


Figure 30. Bipolar Operation with the AD5320

Using AD5320 with an Opto-Isolated Interface

In process-control applications in industrial environments it is often necessary to use an opto-isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur in the area where the DAC is functioning. Opto-isolators provide isolation in excess of 3 kV. Because the AD5320 uses a three-wire serial logic interface, it requires only three opto-isolators to provide the required isolation (see Figure 31). The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a +5 V regulator provides the +5 V supply required for the AD5320.

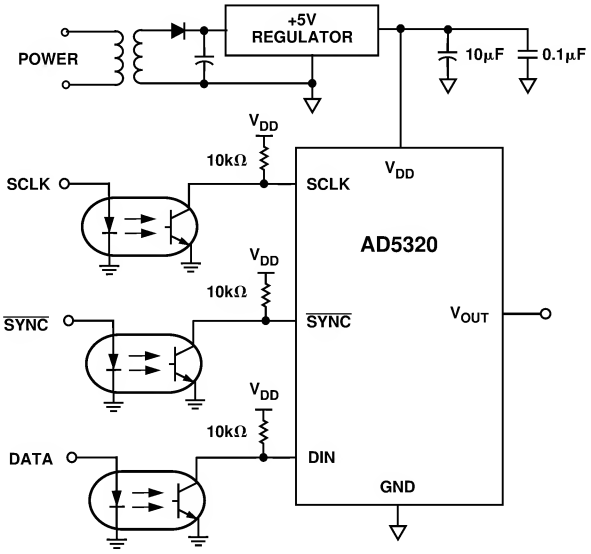


Figure 31. AD5320 with An Opto-Isolated Interface

Power Supply Bypassing and Grounding

When accuracy is important in a circuit it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5320 should have separate analog and digital sections, each having its own area of the board. If the AD5320 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5320.

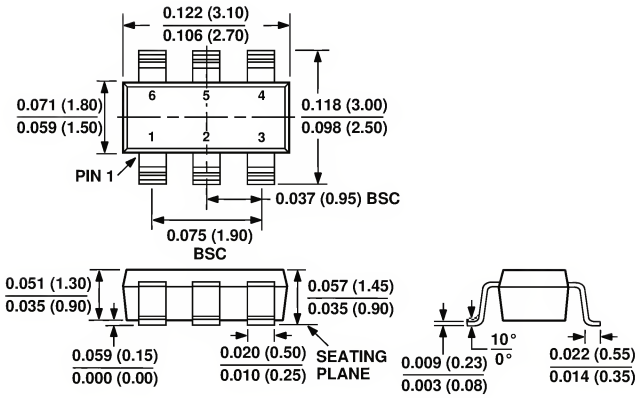
The power supply to the AD5320 should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be physically as close as possible to the device with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitors are the tantalum bead type. It is important that the 0.1 μF capacitor has low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), e.g., common ceramic types of capacitors. This 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.

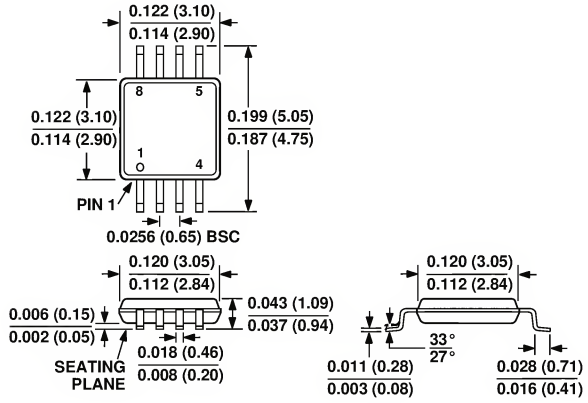
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead SOT-23 (RT-6)



8-Lead microSOIC (RM-8)



C3193–8–12/97

PRINTED IN U.S.A.